REMARKS

Receipt of the Office action mailed March 15, 2004, is acknowledged. Claims 1-3 and 5-9 are pending in the application. Claims 3 and 6-9 have been objected to because of some informalities. Claims 1-3 and 5-9 have been rejected under 35 U.S.C. § 102(b) as being unpatentable over Butts et al., U.S. Patent 5,796,623 ("Butts"). In keeping with the foregoing amendments and the following remarks, claims 1-3 and 5-9 are in condition for allowance.

Claims 3, 5, 6 and 9 have been amended to overcome the objection to the informalities noted in the Office action. Accordingly, the objections to the claims should be withdrawn.

Claims 1-3 and 5-9 have been rejected under 35 U.S.C. § 102(b) as being unpatentable over Butts. Applicants respectfully traverse this rejection.

Claim 1 recites that the MCU communicates data and control signals with respect to the target board through a multiplicity of pins, that the I/O control means selectively outputs RAM address, a specific function register (SFR) address and data outputted from the MCU to the target board and controlling inputted data to the MCU through the multiplicity of pins; and the means for receiving the RAM address, the SFR address and the data through the multiplicity of pins, provides the received data to the target board and controls data to be inputted to the communication means.

Butts does not disclose or even suggest communication through a multiplicity of pins by an MCU, an I/O control means, and a means for receiving the RAM and SFR addresses. Butts discloses an apparatus and method for performing computations, prototyping, execution and simulation using electrically reconfigurable gate arrays

ERCGA logic chips. Butts discloses that reconfigurable blocks are contained in one logic chip, e.g., the Programmable Gate Array PGA made by Xilinx (see col. 7, lines 48-50). As a result, in Butts, each reconfigurable block, e.g., memory block, I/O block, controller and the like, which is tested by the Realizer Hardware System is actually interconnected to each other in the single chip in the Realizer Hardware System.

In contrast, as recited in claim 1, the MCU communicates through a multiplicity of pins with the target board, the I/O control means, and the means for receiving the RAM and SFR addresses. Accordingly, the MCU and the elements that communicate with the MCU are not and cannot be contained on a single chip because they communicate through the multiplicity of pins. Therefore, the present disclosure is directed to some or all of the components of the microprocessor development test board system not being contained on a single chip.

Because Butts does not disclose or even suggest communication through a multiplicity of pins by an MCU, an I/O control means, and a means for receiving the RAM and SFR addresses as recited in claim 1, Butts does not disclose every element of claim 1. Therefore, claim 1 is patentable over Butts and rejection of claim 1, and claims 2, 3 and 5 depending therefrom should be withdrawn.

Claim 6 recites that the MCU is connected to the target board through a multiplicity of first pins for receiving a program codes and providing a program to the target board , and the I/O control means is connected to the MCU chip through a multiplicity of second pins for selecting one of data transmitted through the plurality of first pins in the target board in response to the coded output signals from the decoder.

Butts does not disclose or even suggest that the MCU is connected to the target board through a multiplicity of first pins, and that the I/O control means is connected to the MCU chip through a multiplicity of second pins. As discussed above, Butts discloses an apparatus and method for performing computations, prototyping, execution and simulation using electrically reconfigurable gate arrays ERCGA logic chips. In Butts, each reconfigurable block, e.g., memory block, I/O block, controller and the like, which is tested by the Realizer Hardware System is actually interconnected to each other in the single chip in the Realizer Hardware System.

In contrast, as recited in claim 6, the MCU is connected to the target board through a multiplicity of first pins, and that the I/O control means is connected to the MCU chip through a multiplicity of second pins. Accordingly, the MCU and the I/O control means are not and cannot be contained on a single chip because they communicate through a multiplicity of first pins and second pins. Therefore, the present disclosure is directed to some or all of the components of the microprocessor development test board system not being contained on a single chip.

Because Butts does not disclose or even suggest that the MCU is connected to the target board through a multiplicity of first pins, and that the I/O control means is connected to the MCU chip through a multiplicity of second pins as recited in claim 6, Butts does not disclose every element of claim 6. Therefore, claim 6 is patentable over Butts and rejection of claim 6, and claims 7-9 depending therefrom should be withdrawn.

Applicants further assert that because Butts fails to disclose or even suggest the above-noted elements of claims 1 and 6, Butts cannot support a *prima facie* case of obviousness either individually or in combination with any of the cited references.

Furthermore, as described above, the present disclosure is designed on a board as separate components and is not designed on a single chip. As a result, the disclosed apparatus as claimed can be configured to practically test a plurality of circuits designed in accordance with specific functions. However, the device of Butts can be used only for simulating general purpose logic circuits. In other words, Butts can never be used as a controller, a memory or in any application demanding a particular function. Therefore, Butts also fails to disclose or even suggest that it would be desirable or even possible to provide the claimed apparatus.

Based on the foregoing, Butts cannot support a *prima facie* case of obviousness against claims 1-3 and 5-9. *See In re Sernaker*, 217 U.S.P.Q. 1 (Fed. Cir. 1983) and *Ex Parte Clapp*, 227 U.S.P.Q. 972, 973 (Bd. Pat. App. 1985).

In view of the foregoing, claims 1-3 and 5-9 as presented herein are in good and proper form for allowance. A favorable action on the part of the Examiner is respectfully solicited.

The Examiner is invited to contact the undersigned at the telephone number listed below in order to discuss any remaining issues or matters of form that will place this case in condition for allowance.

Respectfully submitted,

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